

# Low Phase-Noise VCO Design

by

Michael Vogel

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Engineering in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2003

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Author .....

Department of Electrical Engineering and Computer Science

May 9, 2003

Certified by .....

Professor Michael Perrott

Assistant Professor of Electrical Engineering and Computer Science

Thesis Advisor

Certified by .....

Paul Ward

Charles Stark Draper Laboratory

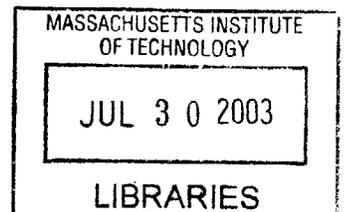
Thesis Supervisor

Accepted by.....

Arthur C. Smith

Chairman, Department Committee on Graduate Students

BARKER





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## Abstract

Draper Laboratory is using a voltage-controlled oscillator (VCO) for mixed-signal processing of a microelectromechanical gyroscope. This thesis studies the design of a new VCO which meets existing circuit specifications with minimal phase noise. An analysis of phase noise sources leads to design guidelines. A single-ended ring-oscillator VCO is then designed at the device level. Devices are sized for optimal performance.

Thesis Advisor: Professor Michael Perrott

Title: Assistant Professor of Electrical Engineering and Computer Science

Thesis Supervisor: Paul Ward

Title: Charles Stark Draper Laboratory



## Acknowledgements

This thesis was prepared at the Charles Stark Draper Laboratory, Inc., under account #15268 GB DLF Support.

Publication of this thesis does not constitute approval by Draper or the sponsoring agency of the findings or conclusions contained herein. It is published for the exchange and stimulation of ideas.

Thanks to: Shida Martinez, Paul Ward, Michael Perrott, Eric Hildebrant, Rob Bousquet

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Michael Vogel

05/09/03

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# Chapter 1 Historical Context and Introduction

Advancements in communication have always been important milestones in history. From the first spoken languages, the transfer and recording of our ideas and memories allowed the next person to continue where our thoughts ended. During the last two centuries, the natural properties of electricity have been harnessed for far and fast communication.

## 1.1 Modern Analog Communications

A physical materialization of signals and an ability to control them is needed for communication. Node voltages are commonly used as signals since devices are modeled in terms of voltages, can be arranged to pass and preserve voltage signals, and can hold voltages with low static power. There is always a relationship between voltage and current, and in several applications currents are better suited to represent signals. Electric signal values can be manipulated with tangible devices such as knobs or levers as was done in early telegraph machines. Today, transistors can adjust electric signals in response to other electric signals in areas and times millions less than can be achieved with human hands. Transistors' size, cost, and speed enabled high-speed communication.

Compared to sound, paper, and mechanical media, electricity has many advantages in carrying information. When carried over metal wires or radiated from an antenna,

electromagnetic waves decay much less than mechanical waves. This allows electric signals to have a further reach than mechanical signals of the same initial power.

Electromagnetic waves can also travel through a vacuum, such as outer space. They propagate faster, but their advantage in communication speed is the rate that data can change.

The time needed for light or sound to travel a short distance often does not matter. A more important metric of communication speed is the quantity of information that can be received over time after communication has begun. In spoken language, this could be limited by how fast one's mouth can change consonant sounds. More generally, this rate is limited by the maximum achievable frequency of the transmitter, medium, and receiver [1]. Even carefully designed mechanical systems tend to heavily dampen signals at frequencies much less than what is commonly used in consumer radios and computers.

High-frequency communication has benefits besides increasing the maximum information rate of one signal. The first benefit is the ability to shift several slow signals to different high frequencies that do not interfere with each other [1]. This allows similar audio signals to be broadcast over different radio stations and received independently. It also allows transmission using antennas with practical physical dimensions. Another benefit is the ability to take more snapshots of a medium-frequency signal [1]. It allows accurate discrete recording of fast changes, as measuring a child's height every month would give more detail about his growth than would measuring his height every year.

## 1.2 Thesis Scope

This thesis will study the design of a voltage-controlled oscillator (VCO) circuit which adjusts the frequency at which the output node's voltage oscillates according to the voltage of the input node. It is designed to be built from one piece of silicon with various chemicals and wires implanted around it, forming mostly transistors. This circuit can be used to match transmitting and receiving frequencies over networks, to set the pace for sequential computational steps, and to tune an antenna to a certain channel [2]. In this setting it will be part of a larger circuit which reads a signal previously shifted to a higher frequency and takes rapid snapshots of this signal. Its design will focus on frequency precision and reliability in its environment. When built and operating, it will consume less power than an insect uses to fly and will be about the size of a period on this paper.

Chapter 2 looks at the operation, mechanisms, and figures of merit of VCO's. Chapter 3 works through the math of measuring frequency precision. It is complicated at first glance, but Table 3.1 summarizes the factors of frequency precision needed for design. Chapter 4 steps through the architecture of the circuit, working from the output backwards. Chapter 5 reexamines each section of the circuit and suggests device sizes. Chapter 6 provides simulation results and recommendations.

## Chapter 2 Voltage Controlled Oscillators

Whenever frequencies in a circuit need to be electrically adjustable, a VCO is used. A VCO is simply a tuner or adjustable clock illustrated in Figure 2.1. VCO's are often used within phase-locked loops (PLL's) to automatically match the frequency of one signal to another. A quick study of oscillators suggests ways of controlling them with a voltage.



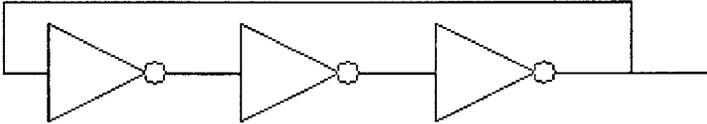
Figure 2.1 VCO Operation

### 2.1 Electrical Oscillation

Crystals such as quartz oscillate due to their chemical configuration and molecular resonances. The crystal may be distorted with large electric fields to change the resonant frequency, but there are more effective ways to make VCO's. Electric resonators such as inductor-capacitor (LC) circuits oscillate by volleying energy between stored magnetic energy and stored electric energy. Capacitance can be controlled with a voltage, but not over a wide range. Also for this thesis, inductors are large unless used for extremely high frequencies, and they cannot be integrated onto silicon at the foundry fabricating this circuit.

A popular oscillator architecture that can be integrated and operates over a wide tuning range is a ring oscillator. It can be modeled as an inverter with unity gain-magnitude whose output is connected back to its input. This creates an unstable feedback loop which rings at a frequency related to the delay of the elements inside the lumped inverter. Ironically, a single inverting amplifier cannot be used since it would be stable at a middle-voltage level. At least three inverting amplifiers are needed to provide enough delay.

The lumped inverter may contain elements beside inverters. For systems with monotonically decreasing magnitude or phase, any open loop gain-magnitude greater than unity at phase less than  $-180^\circ$  leads to instability [3]. This means that ring oscillators could contain filters as well as inverters. However, the simple arrangement of transistors as transconductors makes inverters easy to make, and more phase shift can be achieved per device in an inverter than in a filter. Figure 2.2 shows the basic VCO for this thesis.



**Figure 2.2 Basic Ring Oscillator**

## 2.2 Imperfections

As our models never include all of nature's subtleties, VCO's never behave exactly as predicted. This thesis will focus on irregularities in output frequency, which varies about a uniform value for one input voltage. In the time domain, this is equivalent to timing jitter. This effect is like a metronome whose tempo is not perfectly steady at any one setting. A comparison of ideal and realistic VCO outputs in the time domain is illustrated in Figure 2.3.



**Figure 2.3 Ideal and Real VCO Outputs**

Frequency fluctuations can impair circuits in several ways [2]. In high-bandwidth digital processing, the maximum clock frequency can be limited by uncertainty in the clock used to transfer data instead of propagation delays. In analog-to-digital or digital-to-analog converters, frequency skips can distort signals over time. This is similar to recording a moving object on film which runs at an irregular frames-per-second rate. When played back at a constant rate, the object would appear to move with an additional random component. Likewise, a film recorded at constant speed and played back irregularly would show the same effect. When an oscillator signal is used to demodulate a signal at one channel, a noisy oscillator may not stay tuned to the desired channel. Also, when information is encoded in the phase or frequency of a signal as in several common analog and digital formats, irregular oscillators can send imperfect signals.

## **2.3 Draper Laboratory Specifications**

Draper Laboratory is designing an application-specific integrated circuit (ASIC) for the readout and control of a gyroscope. The gyroscope vibrates at its natural mechanical frequency which changes during operation. Instead of driving the gyroscope at one preselected frequency, Draper Laboratory has chosen to let the gyroscope run at its natural frequency and adjust the electronics according to phase. A VCO within a PLL creates a clock signal in tune with the gyroscope that can be used for demodulation of the gyroscope motion signal, drive of the gyroscope, and clocking of associated converters and digital logic.

Irregularity in the VCO output previously limited gyroscope measurement precision. One objective in the new ASIC design is to minimize VCO frequency randomness. Specifications of the design come from system architecture, available parts, and compatibility with other subcircuits. They are summarized in Table 2-1.

**Table 2-1 Draper VCO Specifications**

Voltage Supplies	GND, 2.5V, 4.25V buffered, 5V
Current Supplies	20 $\mu$ A sink
Power	1mA plus output buffers
Size	Not limited, dominated by large capacitor
Input Range	0-5V
Output Range	0-5V
Tuning Range	2:1
Embedded Low-Pass Filter	Single pole 10kHz
Center Frequency	1.6MHz – 4.8MHz set by external resistor
Available transistors	CMOS, minimum length .6 $\mu$ m
External Parts	One resistor with one end at GND

Other specifications that were not given strict limits but are assumed to be fulfilled by responsible engineering are tuning linearity for PLL dynamics, duty cycle for digital circuits, and consistency over temperature and process variation. Output impedance and available current will be satisfied by using the output buffer from the previous ASIC.

Due to unlimited size, integrated resistors and capacitors can be used. This ASIC will be fabricated on a p-type substrate, so NMOS transistors must have their bodies connected to ground (GND), and bipolar PNP transistors can be made with their collectors connected to GND.

# Chapter 3 Phase Noise

## 3.1 Measurement

To approach the task of minimizing frequency fluctuations, we need a measurable definition of frequency irregularity. We also need a model for predicting its size through other factors. When examining the output of a VCO in the frequency domain, a skirted peak appears. The appearance of this on a spectrum analyzer depends on resolution settings [4]. Traditional, noiseless circuit analysis would predict an impulse at the center frequency so all output power would be focused in an infinitesimally small frequency band. The actual random smearing of output power over a finite bandwidth is called phase noise.

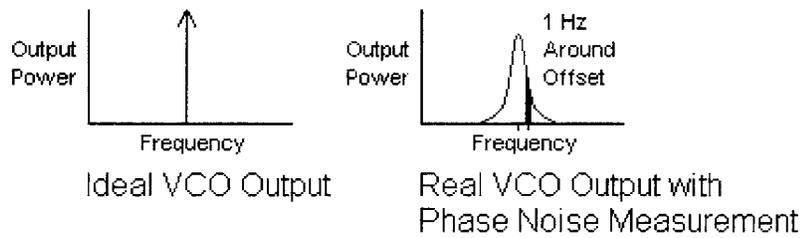


Figure 3.1 Spectral Appearance of Phase Noise

The accepted way of measuring phase noise is to identify a center frequency, choose a single-sided offset frequency, measure the power in a specified bandwidth at that offset, and express that power as a fraction of total oscillator power [5]. As with most noise measurements, this is commonly converted to decibels. This method of measurement is

dual to determining the variance of cycle period in the time domain around a center cycle period.

### 3.2 Noise Sources

The path to phase noise calculation begins with noise sources. Individual devices output random currents and voltages due to vibrations and interactions at the atomic level. Detailed explanations and measurements of these effects are outside the scope of this thesis, and established formulas for various devices will be used. Several models for noisy devices are shown in Figure 3.2. Besides devices, power supplies and the substrate can contribute noise. Their values may change due to changing currents and impedances throughout the entire chip, especially if digital circuits are present. While these changes are not random in the purest definition, they are so numerous and complicated that the most convenient way to model them is as a random process. The substrate of this chip will be connected to ground, and as all other voltages are referenced from ground, we can lump substrate noise into supply noise.

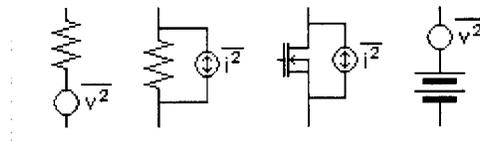


Figure 3.2 Circuit Models for Noisy Devices

As random currents and voltages may change polarity, only their magnitudes are important. This information is captured in mean-square values. If these values can

change to any other random value instantly, their frequency distribution is uniform across all frequencies (white noise). Instead of working with erratic, unrepeatable waveforms in the time domain, engineers can work with flat, consistent noise waveforms in the frequency domain. An infinite spread of noise across frequency suggests infinite power, but there are lower and upper bounds to what is considered and can be measured. White noise is only an approximation in the region being examined. Equations for resistor noise equation 3.1, MOS transistor drain-current noise equation 3.2, and bipolar transistor base-voltage noise equation 3.3 are given below [6].

$$\overline{v^2} = 4kTR\Delta f \quad (3.1)$$

$$\overline{i_d^2} = 4kT \frac{2}{3} g_m \Delta f \quad (3.2)$$

$$\overline{v_b^2} = 4ktr_b \Delta f \quad (3.3)$$

MOS transistors also contribute noise that is not white. Assumed to be caused by surface effects under the oxide, there is a noise term that is inversely proportional to frequency known as flicker noise. It will be ignored since its effects are apparent only in a small region of the VCO output spectrum and do not significantly influence VCO design.

Other non-white noise sources will similarly be ignored.

With appropriate noise sources modeled as mean-square per bandwidth power supplies in series or parallel with each noisy device and supply, the total noise at the output oscillating node can be calculated with standard circuit equations. However, random-variable signals are neither DC (large-signal) nor AC (small-signal). They are all zero-

mean values with a measured variance. Although the units of their standard deviation are voltages and currents, only their variances might add linearly [7]. The variances only add linearly if they are independent, which may not apply to noises from power supplies and shared biases. Furthermore, noise sources may depend on DC bias conditions which are bound to change in parts of an oscillator. These factors are specific to individual circuit configurations.

### 3.3 From Thermal Noise to Phase Noise

#### 3.3.1 Time Variance

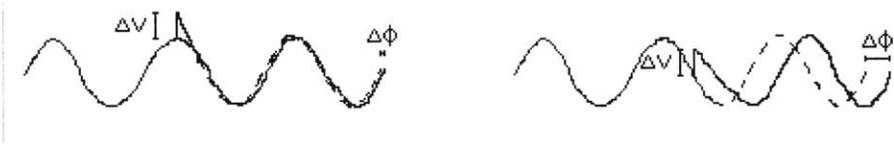
Once the total noise at the oscillating node is calculated, phase noise can be calculated [5]. Noise on the output node can contribute to amplitude noise or phase noise such as in equation 3.4.

$$V_{out}(t) = V_0[1 + A(t)]\cos[\omega_0 t + \phi(t)] \quad (3.4)$$

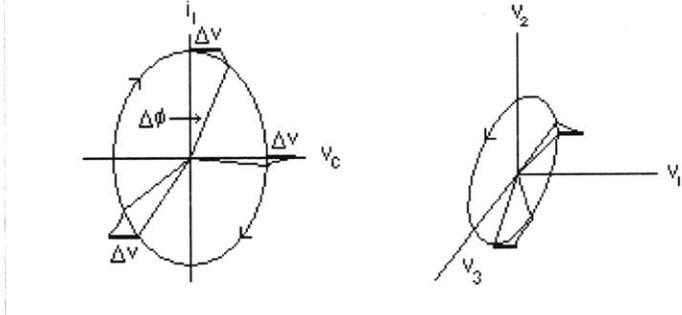
This model is misleading since the two variables  $A(t)$  and  $\phi(t)$  are not truly orthogonal. However, we can assume that the oscillator forces voltages outside of the free-running voltage range back to that range due to nonlinear limits. This allows us to ignore amplitude noise and concentrate only on phase shifts caused by voltage perturbations at the oscillating node.

There is a time dependence on the effect of a voltage perturbation at the output node. The illustrations of voltage jumps at the mid-crossing and peak of the waveform in Figure 3.3 show that phase shifts are more sensitive near mid-crossings. Yet if another

illustration were made with the same voltage jump occurring right after wave's nadir, it would appear that a huge phase shift would result. This is not the case and is due to the loss of amplitude change information in these pictures. Plotting the waveform cycle over the node voltages of the ring oscillator or energy storage elements of a tank oscillator in Figure 3.4 shows how voltage skips contribute to phase skips or amplitude distortions. These state-space plots confirm that output phase is more sensitive to voltage skips near mid-crossings. The angle skips in the state-space diagrams are not exactly the phase skips experienced by the output since the state-space plots are not traced at constant "angular velocity". The VCO design will intentionally have the output move quickly past phase-sensitive regions.



**Figure 3.3 Time-Dependence of Voltage Perturbations to Phase Shifts**

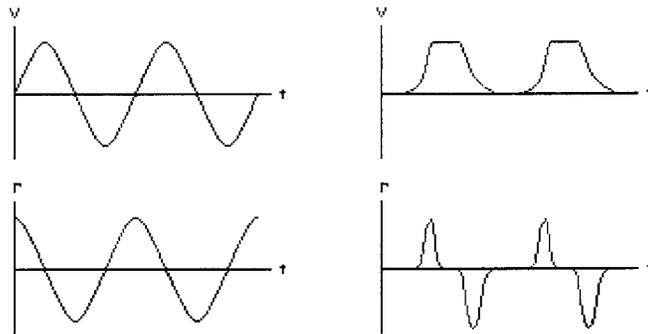


**Figure 3.4 State-Space Diagrams of Voltage Perturbations to Phase Shifts**

A normalized measure of phase sensitivity to voltage perturbations as a function of cycle position is the impulse sensitivity function (ISF) [5]. It linearly relates change in phase to a normalized voltage change as given in equation 3.5.

$$\Delta\phi = \Gamma(\omega_0\tau) \frac{\Delta V}{V_{\max}} = \Gamma(\omega_0\tau) \frac{\Delta q}{q_{\max}} \quad (3.5)$$

Linearity is valid for small voltage changes as can be visualized in previous plots. The ISF can be explicitly calculated by simulating small voltage jumps at different cycle positions and measure consequent phase skips. ISF's for two possible VCO outputs are shown in Figure 3.5.



**Figure 3.5 ISF's for Possible Oscillators**

Since output voltage is going to be the result of charge on a capacitor, normalized node charge is equivalent to normalized node voltage. This allows subsequent calculations to use currents over time instead of volts-per-second which is difficult to conceive and awkward to relate to circuitry.

### 3.3.2 Convolution Including Time-Variance

Given a noise current on a capacitive node, the total phase shift at any time can be measured by summing phase shifts over all previous time with the ISF. This convolution sum is shown in equation 3.6.

$$\phi(t) = \int_{-\infty}^t \frac{\Gamma(\omega_0 \tau)}{q_{\max}} i(\tau) d\tau \quad (3.6)$$

For working with noise at one frequency, it will be useful to find the spectral distribution of the ISF. Since the ISF is periodic at the output frequency, it only has components at multiples of the output frequency including DC.

$$\Gamma(\omega_0 \tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n) \quad (3.7)$$

The total phase-shift convolution integral can be replaced with a linear sum of integrals including the noise current and each component of the ISF spectrum.

$$\phi(t) = \frac{1}{q_{\max}} \left[ c_0 \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0 \tau) d\tau \right] \quad (3.8)$$

The integrals with the product of sinusoidal noise and sinusoidal ISF components are themselves sinusoidal with amplitudes inversely proportional to the difference in frequencies.

$$\int \cos(mx) \cos(nx) dx \approx \frac{\sin(m-n)x}{2(m-n)} \quad (3.9)$$

Total phase will generally be influenced by noise current at a frequency close to a multiple of output frequency.

$$\text{For } i(t) = I \cos(\Delta\omega t) \quad \phi(t) \approx \frac{Ic_0 \sin(\Delta\omega\tau)}{q_{\max} \Delta\omega} \quad (3.10)$$

$$\text{For } i(t) = I \cos[(n\omega_0 + \Delta\omega)t] \quad \phi(t) \approx \frac{Ic_n \sin(\Delta\omega\tau)}{2q_{\max} \Delta\omega} \quad (3.11)$$

The difference between DC offsets and positive frequency offsets arises since offsets can be on either side of a positive frequency.

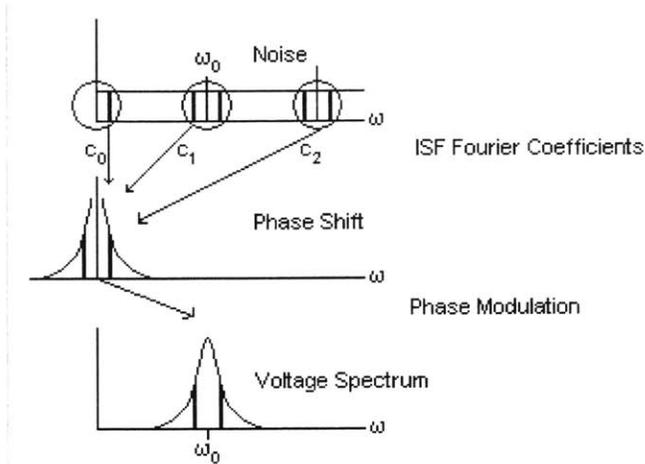
### 3.3.3 Excess Phase Modulation

When this total phase is added to the output frequency, small-angle approximations let it appear as an amplitude modulation of the output voltage.

$$\cos[\omega_0 t + \phi(t)] \approx \cos(\omega_0 t) - \phi(t) \sin(\omega_0 t) \quad (3.12)$$

This shifts the phase due to noise around the output frequency.

For white noise instead of single-tone noise, total phase can be added across all ISF components. The output spectrum at a small offset frequency from the center frequency is the sum of all noise components at that offset from an ISF component. This collection of white noise over multiples of the fundamental frequency is shown in Figure 3.6.

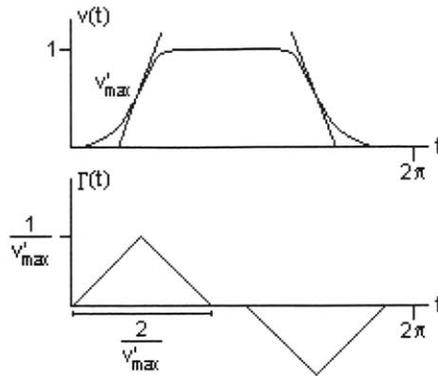


**Figure 3.6 Device Noise to Phase Noise Path**

Since power is related to the square of voltage, and mean-square currents are being used, total power includes the sum of squares of ISF spectrum components. By Parseval's relation, this is proportional to mean-square value of the ISF. Total phase noise in decibels normalized to the output magnitude can be calculated as shown in equation 3.13.

$$L(\Delta\omega) = 10 \log \left( \frac{\overline{i^2} \sum_0^{\infty} c_n^2}{4q_{\max}^2 \Delta\omega^2} \right) = 10 \log \left( \frac{\overline{i^2} \Gamma_{rms}^2}{2q_{\max}^2 \Delta\omega^2} \right) \quad (3.13)$$

If the output waveform is regular and smooth, a convenient approximation can be made of the mean-square value of the ISF. From previous explanations, the ISF is greatest near mid-crossings and is inversely proportional to rise and fall times. A triangular approximation for the ISF derived from a normalized waveform can be used to produce a good estimate of its mean-square value. Geometry gives the mean square ISF value as shown in equation 3.14.



**Figure 3.7 Triangular ISF Approximation**

$$\Gamma_{rms}^2 = \frac{2}{3\pi} \left( \frac{1}{f'_{max}} \right)^3 \quad (3.14)$$

A look at each of the factors in the final VCO phase noise equation suggests design guidelines.

**Table 3-1 Circuit Factors for Phase Noise**

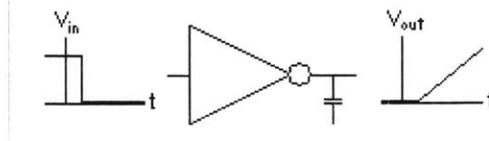
<b>Factor</b>	<b>Circuit Realization to Minimize Phase Noise</b>
$q_{max}^2$	Maximize node capacitors and/or voltage swings
$\Gamma_{rms}^2$	Use fast switching delay cells or inverters
$\frac{\overline{i^2}}{\Delta f}$	Set bias conditions for low noise, use fewer devices

## Chapter 4 General Design

### 4.1 Ring Oscillator Operation

Chapter 2 explained why a ring oscillator will be used. Its architecture consists of a loop with at least unity gain and a total phase shift of one revolution. A mechanical analogy of its operation is repeatedly “doing the wave” in a circular arena. Electrically, active components are needed for unity gain, and inverter configurations produce necessary phase shifts. Along with reasons from chapter 2, inverters are preferable to filters since they have faster switching which lowers phase noise as derived in chapter 3. The basic oscillator structure will be an odd number of inverters connected in a loop.

The abstraction that inverters operate instantly must be broken to understand ring oscillator operation. In steady-state ringing of three inverters, the phase across each inverter must be one third of a revolution instead of one half as an inverter has in isolation. This means that the output of the inverter is retarded in response to the input. Each node has a capacitance, either due to the next input or explicitly added. As each inverter passes and stops a finite current in response to its input voltage, its output voltage is slew-rate limited over the output node capacitance. This effect is illustrated in Figure 4.1. The circuit will ring at the frequency where each inverter’s output slew-rate limit causes a delay of one third of a cycle in response to an equivalent input. This frequency can be controlled by adjusting the current available to each inverter.



**Figure 4.1 Slew-Rate Limited Inverter**

## 4.2 Inverter Design

The first decision in inverter design is selecting between single-ended and double-ended (differential) inverters. Double-ended inverters are often favored in electronics because signal values are only measured as the difference between two nodes. This eliminates shared disturbances such as noise from power supplies or biasing. This would be an advantage in reducing phase noise, but a careful look at the factors of phase noise show a benefit of single-ended inverters [5].

Total charge on the output node is heavily weighted in reducing phase noise. For a given total oscillator current, a double-ended inverter can only pass half as much output node current as a single-ended inverter. To keep an equivalent frequency with half the slew-rate, a double-ended inverter could only have half as much node capacitance as a single-ended inverter. For an equivalent output voltage swing, a double-ended inverter could hold only half as much node charge. In the tradeoff between external noise protection and increased node charge, increased node charge is more beneficial in moderate external noise environments. External noise contributes to node noise more in single-ended inverters, so protection against supply and biasing noise is necessary.

Basic inverters consist of a transistor acting as a transconductor and a load. More elaborate inverters are possible, but they require extra current that is never collected at the output node. In this setting only high gain and fast switching, available output current, and minimal input current are relevant. Loads can be resistors or transistors biased as resistors, but the best choice is an active load of a complementary transistor. This has high gain, low static power, low input current, and requires few parts. Several possible inverters are drawn in Figure 4.2.

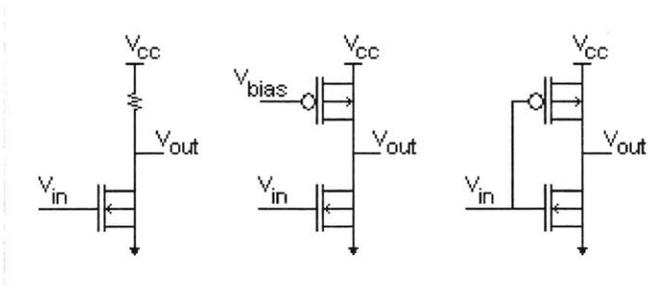
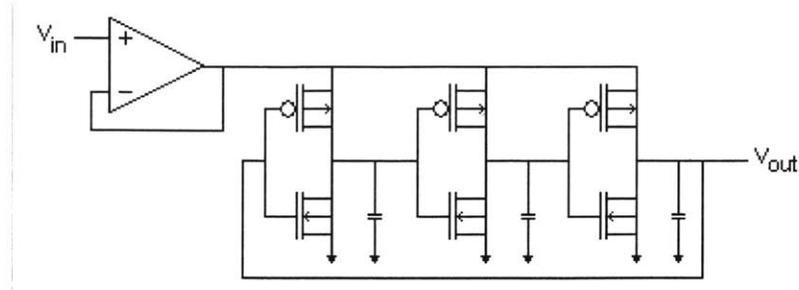


Figure 4.2 Possible Inverters

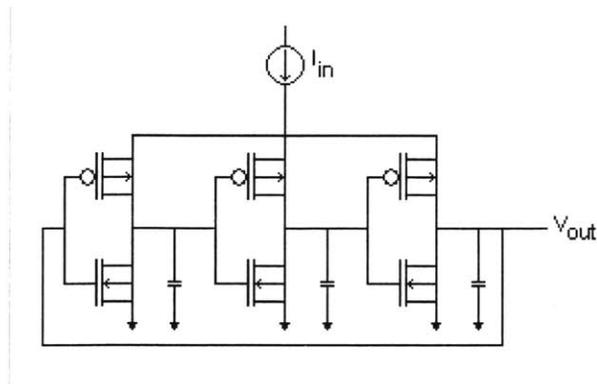
### 4.3 Frequency Control

Complementary MOS (CMOS) inverters cannot be individually biased with a current source, so available current must be controlled indirectly to control frequency. One way to control inverter switching current while protecting against supply noise is by adjusting the voltage spanning all three inverters. This configuration is shown in Figure 4.3. An op-amp designed to supply large currents could use differential gain to reject supply noise while supplying nearly all of its consumed current to inverter nodes. However, a cursory simulation shows that it behaves nonlinearly and fails to achieve the necessary 2:1 tuning range over the entire 3:1 center-frequency range.



**Figure 4.3 Possible Frequency Control Scheme**

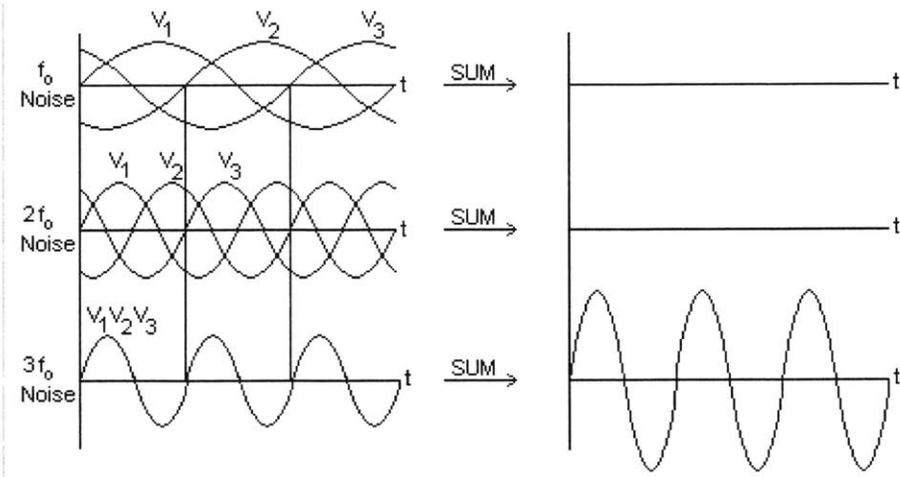
While individual CMOS inverters cannot be current biased, several CMOS inverters can share a common current bias as shown in Figure 4.4. At any given moment they will not pass the same amount of current, but if they are identical they will pass the same average current. The voltage at the node connecting the inverters to their current bias will change to accommodate changing current. It will also have a small ripple to accommodate momentary asymmetry in inverter current.



**Figure 4.4 Current-Controlled Oscillator**

This method of controlling output frequency with available current is direct and linear. Output frequency is related to inverter slew rate, which is defined by available current.

Another benefit in this structure comes from the equal phase shifts each inverter adds. The noise currents from biasing on each inverter node are not independent. Coming from a common source, their phases relative to output shift equally around one revolution when collecting on inverter nodes. This shifts the corresponding ISF for each node by the same phase. The resulting sum of all nodes' phase effects is nonzero only for noise frequencies at a multiple of the number of inverters times the output frequency. This can be illustrated for any number of inverters, for three in Figure 4.5, but is easier to visualize with an inverter in isolation. A noise signal added to the input and output shifted by an entire cycle would result in destructive interference as the inverted input would cancel the output noise. A similar noise signal shifted by half a cycle would result in constructive interference as the inverted input would double the output noise.



**Figure 4.5 Effect of Correlated Noise Sources**

This effect suggests that a higher number of inverters improves phase noise. However, gains here would come at the cost of smaller capacitors at each node. Generally, every improvement with increased number of stages, such as better ISF from relatively less

switching, is canceled. The prices of more inverters are as many more nodes contributing to phase noise, and adjustments needed to keep the same frequency and total current. Some effects such as flicker and external noise contributions may depend on the number of inverters [5]. Still, with little overall dependence on inverter number, design factors such as size, simplicity, and matching suggest using the minimum number, three.

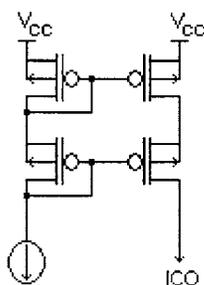
## **4.4 Supply Noise Rejection**

The input to the current-controlled ring oscillator (ICO) must be protected from supply noise. The input is sourced from a voltage higher than the ICO from the constraint that the circuit is fabricated on a p-substrate. NMOS transistors will have their bodies grounded, and to avoid body effects NMOS transistors should have their sources connected to ground whenever possible. This requires the inverters to be connected to GND instead of the top rail. The input current to the ICO will come from a PMOS current mirror connected to the high voltage rail. As that rail's voltage changes randomly, the current to the ICO should remain constant with the current mirror's input current and ICO input voltage. This requires a high output impedance from the current mirror.

### **4.4.1 Cascodes**

With plenty of voltage headroom, an effective way to increase mirror output-impedance is with a cascode [6]. Another PMOS transistor can be added in series with the mirror output. Usually cascode gates are connected to a constant voltage, but this cascode is

effectively referenced from the high voltage rail, not ground. The desired cascode effect is only achieved if the gate of the cascode transistor is connected to a voltage that changes with the high rail voltage. This is easily arranged with a second diode connection before the current mirror input as shown in Figure 4.6.

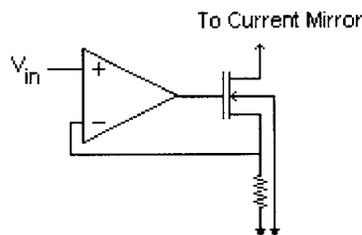


**Figure 4.6 Cascode with Rail-Controlled Bias**

The cascode arrangement increases output resistance as follows, referring to an increase in rail voltage. As the drain-to-source voltage magnitude of the cascode transistor increases, output current increases according to its output resistance. This increased current also passes through the original mirror-output transistor, whose drain-to-source voltage magnitude must increase as its gate-to-source voltage is constant. As the node connecting the two output transistors decreases in voltage, output current is suppressed through the lower gate-to-source voltage magnitude and transconductance of the cascode transistor. The overall benefit of the cascode is an increase in output resistance by a factor of the output resistance and transconductance product of the cascode transistor.

#### 4.4.2 High Impedance V-to-I Converter

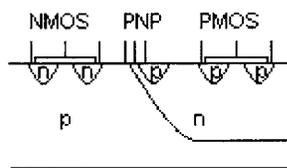
This biasing arrangement assumed that the mirror input current would remain constant over supply voltage change. Also, circuit specifications demand that center frequency, here center current, should be set with an external resistor with one end at ground. A transistor with high output resistance is a good starting point for supply constant current over changing output voltage. Unless another mirror is made to redirect current, an NMOS transistor with its source voltage at the external resistor voltage is necessary. It remains the best choice as the extra mirror would be wasteful in parts, power, and noise. High-gain feedback can be used to control the external resistor voltage, and therefore current. It also increases the output resistance of the NMOS transistor by the op-amp gain and NMOS transconductance product.



**Figure 4.7 High Output Impedance V-to-I Converter**

Keeping in mind that any op-amp consists of many active devices, this op-amp should be tailored to its purpose here. No output current is drawn, so high-current output buffer stages are not necessary. Similarly, the VCO input rate of change (FM bandwidth) will be limited to 10 kHz, so high frequency gains are not important. All that is needed is high gain.

The rest of the circuit design generally does not affect phase noise. One final part that could be the voltage buffer used in shifting the VCO input range to a suitable one for the external resistor. Source-followers are effective buffers as they have low output impedance. This is needed to preserve a buffered voltage with changing supply voltage and other noise. Low output impedance comes from high transconductance which would be even higher if a bipolar transistor were used. Fortunately, on a p-substrate, a PNP bipolar transistor with the collector at ground can be made on a CMOS process as illustrated in silicon in Figure 4.8. This can be used to make a buffer with better supply noise rejection.



**Figure 4.8 PNP Bipolar Transistor on CMOS Process**

## Chapter 5 Specific Design

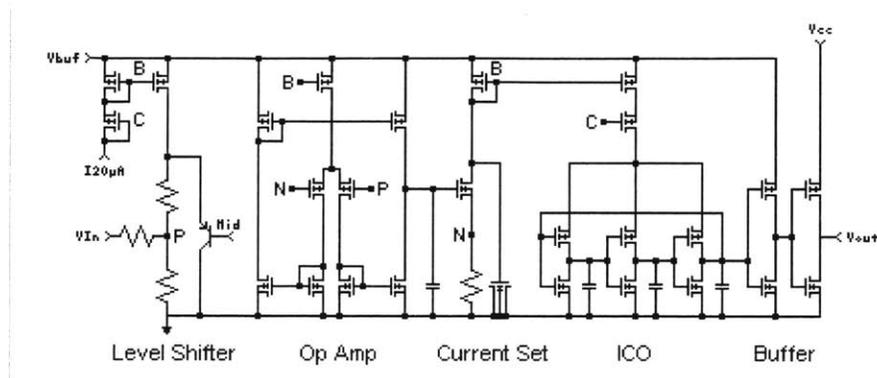


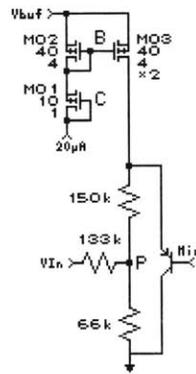
Figure 5.1 Total VCO Schematic

The design for minimum phase noise started at the oscillator and went backward. For clarity, the implementation details will start at the input and go forward. With several voltage rails available, the buffered 4.25 V (V<sub>buf</sub>) rail is used in all supply-noise sensitive parts of the circuit. The final output is switched to the 5 V (V<sub>cc</sub>) rail to satisfy the output swing specification. Ground (GND) is the end of all current paths in the circuit except for the 2.5 V (Mid) rail in the level-shifter. The resistor connected between node N and GND is the external, center-frequency setting resistor.

### 5.1 Level Shifter

There is a node designated for connection to a 20 μA current sink elsewhere on the ASIC. This current is mirrored for biasing throughout the VCO. When multiplying or dividing

current with a MOS current mirror, it is best to keep lengths equal for matching over fabrication variation and higher order effects [6]. Since transistors mirrored to M02 will need high output resistance, M02 has a length of 4  $\mu\text{m}$ . Looking ahead in the circuit, the ICO input cascode transistor needs a gate bias that moves with the supply voltage. Another diode connection in the neighboring leg, under the current mirror input, might encroach the adjacent transistors' active operation at high current levels. With plenty of headroom available under M02, M01 is sized to be small and create an appropriate gate bias for the ICO input cascode transistor.



**Figure 5.2 Mid-Buffer and Level-Shifter**

The emitter of the PNP transistor is the buffered MID voltage. It is no longer at 2.5 V, but all that matters is its consistency. The current mirror supplies 40  $\mu\text{A}$  to the PNP transistor, enough to keep it active regardless of up to 15  $\mu\text{A}$  going to the adjacent resistor network. The high output impedance of M03 compared to the low impedance into the emitter of the PNP transistor provides enough supply noise protection that a cascode is not necessary. Supply noise effects here are much less than supply noise

effects further in the circuit. The resistors are sized to shift an input voltage ( $V_{In}$ ) with a range of 0-5 V to 1-2 V at node P (non-inverting op-amp input). They are sized large to minimize currents.

## 5.2 Op-Amp

M04 through M12 make a high-gain op-amp. The level-shifted input is at PIN, and the inverting input is connected to the external resistor at N. The op-amp uses the transconductance of both inputs by circulating them to draw against the output resistances of M12 and M10. While transconductance increases with bias current, output resistance decreases more. M05 and M06 are sized for large transconductance, but low currents everywhere create high gain. M08 and M09 are sized for low transconductance to drive M07 and M10 with larger gate voltage change. M12 and M10 are sized for high output resistance, while ensuring a sufficient output voltage swing to drive the following NMOS transistor. A capacitor is added at the output for dominant pole compensation with the parallel output resistances of M12 and M10. This prevents high frequency instability.

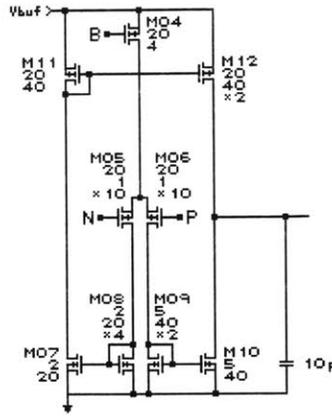
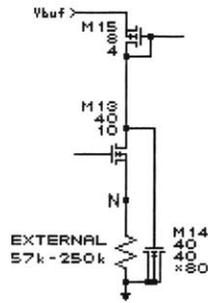


Figure 5.3 Low-Power High-Gain Op-amp

### 5.3 V-to-I Converter

M13 is an NMOS transistor with its source voltage higher than its body voltage. It also requires high output resistance and high transconductance to reject supply noise within its feedback loop. M13 needs to be large in both width and length to satisfy all these requirements. While a goal was to supply as much available current as possible to the ring oscillator, the external resistor must be reasonably sized and current mirrors cannot accurately provide very high gain. The current mirror gain is chosen to be 20 as a compromise, and M15 is sized small to allow easy multiplication.



**Figure 5.4 Voltage-to-Current Converter and Low-Pass Filter**

The low-pass filter required in this VCO was placed at a bad location. During design, between M13 and M15 seemed like a good place for it. It was close to the ring oscillator to reject earlier high-frequency noise, and the parallel resistances of M13 and M15 could be made large. However, instead of being in series with the ICO current mirror, it is in parallel defeating the purpose of the high-resistance M13 configuration. Instead of only preventing high-frequency signals from early circuit stages from continuing, the filter also allows high-frequency supply noise signals to pass through the ICO current mirror and be mirrored. This should not be devastating as the ICO is only sensitive to noise at triple-multiples of its center frequency which are coupled to rapidly decreasing triple-multiple ISF Fourier coefficients. Noise near DC is still heavily rejected.

## **5.4 Current-Controlled Oscillator**

The benefits of the cascode for supply noise rejection had factors of output resistance of the mirror output transistor, and transconductance and output resistance of the cascode transistor. M16 and M17 are sized to achieve high total output resistance while remaining active as the ICO input's voltage is greater than the oscillating voltage swing.

The PMOS and NMOS transistors in the ICO are scaled for symmetric rise and fall times. Their different sizes are due to differences in p and n carrier mobility. They have high transconductances to benefit switching speed. For a switching input, a higher transconductance supplies or sinks current to the output node capacitor faster. At the time of design, their immediate proximity to oscillating nodes raised concern of being sized to create too much device noise. This concern was unfounded, and they should be shorter with higher transconductances. The ICO capacitors are sized to achieve the desired frequency with available current.

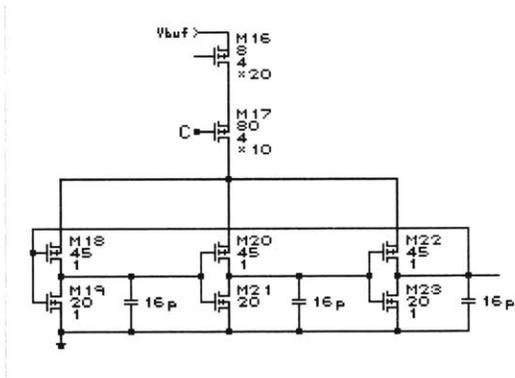


Figure 5.5 ICO with Cascoded Input

## 5.5 Output Stage

The output buffers in Figure 5.6 are identical to the earlier Draper Laboratory ASIC to match output specifications. First there is an inverter without an explicit load capacitor to generate a faster switching signal. It is sized to switch at an input of half the ring oscillator swing. This swing is not uniform over frequency, so duty cycle will change

slightly with frequency. Finally there is a large inverter to supply output current with a 0-5 V swing.

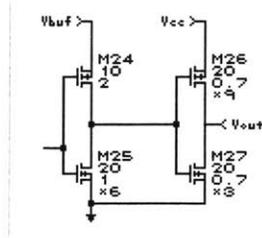


Figure 5.6 Output Buffers

## Chapter 6 Conclusions

### 6.1 Phase Noise Estimate

Circuit values can be inserted into equation 3.13, developed by Ali Hajimiri, for a phase noise estimate. While this circuit will not be measured before the completion of this thesis, a previous VCO was predicted and tested using equation 3.13. The expectation was about 8 dB optimistic which is reasonable since some noise sources were ignored.

Summing noise signals throughout the circuit at its biases gives a current variance per unit frequency of  $1.96 \times 10^{-22} \text{ A}^2 / \text{Hz}$ . Running a transient simulation on HSPICE, normalizing one cycle, and using the estimate in equation 3.14 produces a mean-square ISF value of .2732. The ring oscillator swing from the transient simulation is also used to find the maximum node charge which is  $3.33 \times 10^{-11} \text{ C}$ . These values can be plugged into equation 3.13 along with any offset frequency within the range where  $1/f$  noise and the noise floor are inconsequential. Figure 6.1 shows phase noise estimates using equation 3.13.

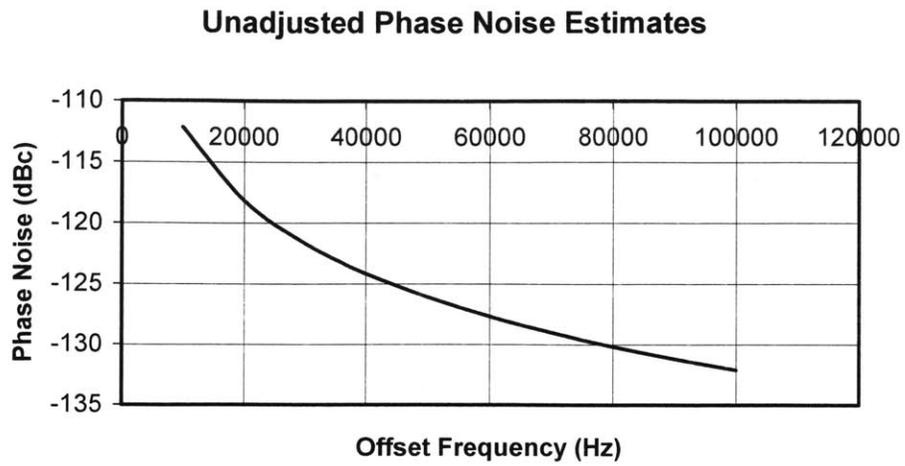


Figure 6.1 Phase Noise Estimates

## 6.2 Other Simulations

Transient simulations show that the VCO is expected to work well. The VCO was simulated at different center frequencies, temperatures, process variations, and Vcc voltages. Simulation results are summarized in the following table.

**Table 6-1 Circuit Simulation Results**

Nominal Frequency for Sims	3.2 MHz	
Supply Current	360 $\mu$ A plus output buffers	
Tuning Range	+33%, -39%	
Tuning Gain Linearity	4.1% ppk residuals / nominal	
Tuning Gain Dynamic	34% ppk residuals / nominal (temperature and process)	
Duty Cycle	45%	
Frequency VCC sensitivity	2.5% / V	
External Resistor Values	Center Frequency (MHz)	Resistor Value (k $\Omega$ )
	1.6	250
	2.2	168
	3.2	104
	3.6	88
	4.8	57

The exact values in this table are only for the center frequency listed. Changes over operating point can be predicted and observed in simulation. For power, the currents in the buffer and op-amp are fixed, while the currents through the external resistor and ICO vary linearly with external resistance and input voltage. Due to nonlinearity in the ICO, tuning range varies slightly with bias conditions. The design ensures a 2:1 ratio across the required range, but this increases slightly at lower frequencies. Tuning gain linearity and dynamics remain similar, although the actual slope gauged by the linearity changes as described. The internal voltage swing of the ICO changes with ICO current due to finite output resistances and transconductances. With unchanging output buffers, the buffers will not switch at exactly the same phase of a changing internal ICO swing. This

results in a duty cycle which increases slightly with bias frequency, as internal ICO swing increase with ICO current.

### **6.3 Future Recommendations**

Even with cascodes, AC simulations with 10 mV peak supply noise show that the noise at each node of the ICO is dominated by supply noise. The low-pass filter should have been placed so that it would not introduce high-frequency supply noise signals into the signal path. Also, the ICO inverters should have been faster without concern for device noise including short channel effects. A length reduction to .6  $\mu\text{m}$ , or a width or multiplicity increase of 8x on each transistor would each allow a 20% larger capacitor on each node. This would translate to 20% less phase noise.

More accurate VCO's may arise in the future in many ways. As more metals and materials are being implanted in integrated circuits, integrated LC circuits may become common. Ring oscillators may be replaced entirely with tank oscillators. Low noise environments could be created with advancements in layout and digital design on chips with both analog and digital circuitry. Better characterization of flicker noise would allow a more thorough analysis of circuit noise. All of these areas of study contribute to better communication.

## Bibliography

- [1] Alan V. Oppenheim and Alan S. Willsky. *Signals & Systems*. Prentice Hall. Upper Saddle River, NJ, second edition. 1997.
- [2] Todd Charles Weigandt. *Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay Cell Based VCO's and Frequency Synthesizers*. 1998.
- [3] Kent Lundberg. *6.302 Class Notes at Massachusetts Institute of Technology*. 2002.
- [4] Hewlett-Packard Company, Loveland, CO. *Operating Manual Model 3585A Spectrum Analyzer*. 1978.
- [5] Ali Hajimiri and Thomas H. Lee. *The Design of Low Noise Oscillators*. Kluwer Academic Publishers. Norwell, MA. 1999.
- [6] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Inc. New York. 2001.
- [7] Dimitri P. Bertsekas and John N. Tsitsiklis. *Introduction to Probability*. Athena Scientific. Belmont, MA. 2002.